UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,866	11/27/2001	Amit Dinesh Sanghani	SUN-P5759	4848

7590 02/24/2004

DANIEL VAUGHAN
PARK, VAUGHAN & FLEMING LLP
702 MARSHALL STREET
SUITE 310
REDWOOD CITY, CA 94063

EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/996,866	Applicant(s) SANGHANI, AMIT DINESH	
	Examiner David Ton	Art Unit 2133	

-- The MAILING DATE of this communication appears on th cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-22 are presented for examination.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Eccles patent no. 6,574,758.

4. As to claim 1, Eccles teaches the invention substantially as claimed, including a double data rate (DDR) circuit [see Fig. 2], comprising:

> A stimulus generator [test signal generator 9 of Fig. 2] configured to generate a test DDR signal [col. 1 lines 29-39];
> An evaluator [comparator 11 of Fig. 2] configured to compare said test DDR signal with a response signal produced by the DDR circuit in response to said test DDR signal [see claim 1]; and
> A result generator configured to generate an error condition if said response signal does not have a predetermined relationship to said test DDR signal [see claim 1].

Eccles does not explicitly teach a self testable DDR circuit in the implementation of Fig. 2; however, in a similar implementation of Fig. 4 [see Fig. 4], Eccles teaches that

Fig. 4 is built into an ASIC chip [see col. 6 lines 39-43]. Another word, this ASIC chip includes a built-in self-test (BIST) DDR circuit.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to provide a self testable DDR circuit by implement the teachings of Eccles into ASIC chip as suggested by Eccles. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a built-in self-test (BIST) for a semiconductor device.

5. As to claim 2, Eccles teaches the stimulus generator, the evaluator and the result generator are located on a single semiconductor chip [col. 6 lines 39-43].

6. As to claim 3, Eccles teaches the self testing perform without crossing a boundary of the semiconductor chip [Fig. 4 implemented in an ASIC, col. 6 lines 39-43] thereby allowing said self test to be performed at an on-chip clock speed [clock 1 and clock 2 of Fig. 4].

7. Claims 4-8 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Eccles patent no. 6,574,758 in view of Nadeau-Dostie et al. (Nadeau-Dostie) patent no. 5,349,587.

8. As to claim 4, Eccles does not teach the stimulus generator comprises a linear feedback shift register. A self test mode control by a BIST controller

Nadeau-Dostie teaches a BIST including a test stimulus generator comprises a linear feedback shift register [col. 5 lines 33-57]

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to implement the test signal generator as taught by Eccles with a linear feedback shift register as taught by Nadeau-Dostie. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a simple circuit for the test generator.

9. As to claim 5, Nadeau-Dostie teaches a self-test mode operation controlled by a BIST controller [col. 5 lines 33-57].

10. As to claim 6, Nadeau-Dostie teaches response rate same as the rate of a normal mode of operation [see claim 2, 3 and 7].

11. As to claim 7, Nadeau-Dostie teaches performing said comparison dynamically as said response signal is generated [see claim 4].

12. As to claim 8, Eccles and Nadeau-Dostie do not teach the result generator maintain the error condition during generation and evaluation of subsequent test DDR signal.

Official Notice is taken that maintain the error condition during generation and evaluation of subsequent test signal is well known in the art. There are 3 options when running a test program: continue on fail (with the fail light is ON), stop on fail or restart on fail. Maintain the error condition while running a subsequent test signal is a continue on fail option.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to implement the self-test taught by Eccles and Nadeau-Dostie in a continue on fail option. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would provide a simple diagnostic procedure.

13. Claims 9-10, 17 and 20 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Eccles patent no. 6,574,758 in view of Johnson et al. (Johnson) patent no. 5,023,590.

14. As to claims 9, 17 and 20, Eccles teaches the invention substantially as claimed, including a self testable double data rate (DDR) circuit [see Fig. 4] for I/O interface [interface between first circuit and second circuit of Fig. 4], comprising a signal generator [test signal generator 9 of Fig. 2]; an evaluator [comparator 11 of Fig. 2]; a result generator [see claim 1] located on a single semiconductor chip [col. 6 lines 39-43] as discussed in claim 1 above.

However, Eccles does not teach the DDR circuit is configured with macro cell.

Johnson teaches a cascadable 17-bit self-testing comparator [see Fig. 1 and claim 1] by interconnecting the data pins with the logic macro cells for fast comparison of 17-bits on chip [see col. 1 lines 5-10].

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to configure the DDR circuits taught by Eccles as with macro cell as taught by Johnson. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a fast DDR built-in self-test circuit.

15. As to claim 10, Eccles teaches the testing of the I/O interface is perform without the I/O pattern crossing a boundary of the semiconductor chip [col. 6 lines 39-43],

thereby allowing said testing to be performed at an on-chip clock speed [clock 1 and clock 2 of Fig. 4].

16. Claims 11-16, 18-19 and 21-22 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Eccles patent no. 6,574,758 in view of Johnson et al. (Johnson) patent no. 5,023,590 and further in view of Nadeau-Dostie et al. (Nadeau-Dostie) patent no. 5,349,587.

17. As to claim 11, Eccles and Johnson do not teach the generator comprises a linear feedback shift register.

Nadeau-Dostie teaches a BIST including a test stimulus generator comprises a linear feedback shift register [col. 5 lines 33-57]

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to implement the test signal generator as taught by Eccles with a linear feedback shift register as taught by Nadeau-Dostie. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would provide a simple circuit for the test generator.

18. As to claim 12, Eccles, Johnson and Nadeau-Dostie do not teach a linear feedback register has a characteristic polynomial of x10 + x3 + 1.

Official Notice is taken that a linear feedback register has a characteristic polynomial of x10 + x3 + 1 is well known in the art.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to implement the test signal generator as taught by Eccles with a linear feedback shift register has a characteristic polynomial of x10 + x3 + 1. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would provide a simple circuit for the DDR test generator.

19. As to claim 13, Nadeau-Dostie teaches performing said comparison in real time [see claim 4].

20. As to claim 14, Nadeau-Dostie teaches test data form at a first data rate in normal operation mode and produces the output at said first data rate in a self-testing mode [see claim 2, 3 and 7].

21. As to claims 15&16, Johnson teaches an I/O interface macro cell [see claim 1].

22. As to claim 18, Johnson teaches an I/O interface comprising a built-in self-test controller [programmable crossbar switch 22 of Fig. 1] to control said self testing of said I/O macro cell and said clock macro cell [see claim 1].

23. As to claim 19, Johnson teaches the self-testing of each macro cell is performed at an operational speed of said macro cell [inherently on col. 4 lines 1-15].

24. As to claim 21, Eccles teaches the stimulus generator, the evaluator and the result generator are located on a single semiconductor chip [col. 6 lines 39-43].

25. As to claim 22, Eccles teaches the self testing perform without crossing a boundary of the semiconductor chip [Fig. 4 implemented in an ASIC, col. 6 lines 39-43] thereby allowing said self test to be performed at an on-chip clock speed [clock 1 and clock 2 of Fig. 4].

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DT

February 20, 2004

DAVID TON
PRIMARY EXAMINER